**“A Huge Microworld” (English, grades 10-11)**

**Glossary**

**A**

**Anti-static tweezers** *(Антистатические пинцеты)*
Tools to handle microchips without static damage.

**Annealing** *(Отжиг)*
Heating process to repair silicon crystal structure.

**ASIC (Application-Specific IC)** *(Заказная ИС)*
A chip designed for a single purpose (e.g., Bitcoin mining).

**B**

**Bonding wire** *(Контактный провод)*
Thin wire connecting a microchip to its package.

**BGA (Ball Grid Array)** *(Массив шариковых выводов)*
Chip packaging with solder balls underneath.

**Bipolar transistor** *(Биполярный транзистор)*
Fast-switching transistor type.

**C**

**Cleanroom** *(Чистая комната)*
Sterile environment for chip manufacturing.

**Capacitor** *(Конденсатор)*
Stores electrical charge in circuits.

**CMOS (Complementary MOS)** *(КМОП-технология)*
Low-power transistor technology used in CPUs.

**D**

**Die (Microchip die)** *(Кристалл микросхемы)*
The tiny silicon piece containing the circuit.

**DRAM (Dynamic RAM)** *(Динамическая память)*
Volatile memory used in RAM modules.

**Doping** *(Легирование)*
Adding impurities to silicon to alter conductivity.

**E**

**Etching** *(Травление)*
Process to remove material for circuit patterns.

**EPROM (Erasable PROM)** *(Стираемое ПЗУ)*
Old-school reprogrammable memory.

**Electromigration** *(Электромиграция)*
Metal degradation in chips due to current.

**F**

**Fab (Fabrication plant)** *(Фабрика полупроводников)*
Factory where microchips are made.

**FinFET** *(Транзистор с ребристым затвором)*
3D transistor design for modern chips.

**Flip-chip** *(Перевёрнутый кристалл)*
Packaging where the die faces downward.

**G**

**Graphene** *(Графен)*
Ultra-thin material for future chips.

**GDSII (Graphic Data System)** *(Формат GDSII)*
File format for chip design layouts.

**H**

**Hybrid circuit** *(Гибридная схема)*
Combines silicon chips with other components.

**High-κ dielectric** *(Диэлектрик с высоким κ)*
Insulating material for advanced transistors.

**I**

**Integrated Circuit (IC)** *(Интегральная схема)*
A complete electronic circuit on a single chip.

**Interposer** *(Интерпозер)*
Layer connecting multiple chips in a package.

**Ion implantation** *(Ионная имплантация)*
Shooting ions into silicon to change its properties.

**J**

**Jumper** *(Джампер, перемычка)*
Tiny connector to close/open circuits.

**JEDEC (Joint Electron Device Council)** *(JEDEC-стандарт)*
Industry group setting chip standards.

**K**

**Known Good Die (KGD)** *(Исправный кристалл)*
Pre-tested microchip die before packaging.

**KGD test handler** *(Тестер кристаллов)*
Machine for testing unpackaged dies.

**L**

**Lithography** *(Литография)*
Printing circuit patterns on silicon.

**LGA (Land Grid Array)** *(Массив контактных площадок)*
Chip packaging with flat contacts (used in Intel CPUs).

**M**

**Microcontroller** *(Микроконтроллер)*
Small computer on a single IC (e.g., in toys).

**Moore’s Law** *(Закон Мура)*
Prediction that transistor counts double every 2 years.

**N**

**Nanometer (nm)** *(Нанометр)*
Unit for chip feature sizes (e.g., 3nm process).

**NAND flash** *(NAND-память)*
Storage in SSDs and USB drives.

**O**

**Oxidation** *(Окисление)*
Creating silicon dioxide layers on wafers.

**Optical inspection** *(Оптический контроль)*
Camera-based defect detection.

**P**

**Photomask** *(Фотошаблон)*
Template for circuit patterns in lithography.

**PCB (Printed Circuit Board)** *(Печатная плата)*
Board connecting chips and components.

**Q**

**Quality Control (QC)** *(Контроль качества)*
Testing chips for defects.

**Quantum dot** *(Квантовая точка)*
Nanoscale semiconductor for future displays/chips.

**R**

**Resistor** *(Резистор)*
Limits electrical current.

**Reticle** *(Ретикул)*
Smaller version of a photomask.

**S**

**Semiconductor** *(Полупроводник)*
Material (e.g., silicon) used for chips.

**SOIC (Small Outline IC)** *(Корпус SOIC)*
Common surface-mount chip package.

**T**

**Transistor** *(Транзистор)*
Building block of modern electronics.

**TSV (Through-Silicon Via)** *(Сквозной кремниевый контакт)*
Vertical connection in 3D chips.

**U**

**UV Light** *(Ультрафиолетовый свет)*
Used in lithography and sterilization.

**Underfill** *(Подложка)*
Epoxy protecting solder joints in chips.

**V**

**Via** *(Вайа, межслойное соединение)*
Tiny hole connecting chip layers.

**VLSI (Very Large-Scale Integration)** *(СБИС, сверхбольшая ИС)*
Designing complex ICs with millions of transistors.

**W**

**Wafer** *(Кремниевая пластина)*
Thin silicon disk for chip production.

**Wire bonding** *(Проводной монтаж)*
Attaching wires to chip contacts.

**X**

**X-ray inspection** *(Рентгеновский контроль)*
Detects hidden defects in chips.

**XOR gate** *(Логический элемент XOR)*
Basic digital logic component.

**Y**

**Yield** *(Выход годных)*
Percentage of defect-free chips per batch.

**Yield enhancement** *(Повышение выхода годных)*
Techniques to reduce defects.

**Z**

**Zener diode** *(Стабилитрон)*
Diode for voltage regulation.

**Zero-ohm resistor** *(Резистор 0 Ом)*
Used as a "wire" in PCB designs.